IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) An apparatus comprising:

~~an~~ a CMOS amplifier;

a CMOS gain circuit coupled to an output of the CMOS amplifier, the CMOS gain circuit to provide at least two gain values in response to the output of the CMOS amplifier; and

a control circuit to provide one of the at least two gain values as an output.

2. (Currently Amended) The apparatus as claimed in claim 1, wherein the CMOS gain circuit includes at least two equalization circuits each providing a respective one of the at least two gain values.

3. (Currently Amended) The apparatus as claimed in claim 2, wherein the at least two equalization circuits are coupled in series to the output of the CMOS amplifier.

4. (Currently Amended) The apparatus as claimed in claim 2, wherein each of the at least two equalization circuits includes an RC filter.

5. (Original) The apparatus as claimed in claim 4, wherein a resistance R and a capacitance C of the RC filter are implemented using on-chip components.

6. (Original) The apparatus as claimed in claim 4, wherein a resistance R of the RC filter is implemented using passive components.

7. (Original) The apparatus as claimed in claim 4, wherein a resistance R of the RC filter is implemented using active components.

8. (Original) The apparatus as claimed in claim 4, wherein all resistors in the apparatus are formed of a same technology.

9. (Original) The apparatus as claimed in claim 8, wherein the same technology is a poly resistance technology

10. (Original) The apparatus as claimed in claim 4, wherein R and C values of the RC filter are fixed during a circuit design phase.

11. (Canceled)

12. (Currently Amended) The apparatus as claimed in claim 11, wherein the CMOS gain circuit includes at least two equalization circuits each providing a respective one of the at least two gain values.

13. (Currently Amended) The apparatus as claimed in claim 12, wherein the at least two equalization circuits are coupled in series to the output of the CMOS amplifier.

14. (Currently Amended) The apparatus as claimed in claim 13, wherein each of the at least two equalization circuits includes an RC filter.

15. (Original) The apparatus as claimed in claim 1, wherein the control circuit includes a DC feedback circuit and the output provided by the control circuit is selected in response to the DC feedback circuit.

16. (Original) The apparatus as claimed in claim 15, wherein the DC feedback circuit uses DC balance to help select the output.

17. (Currently Amended) A system comprising:

a transmitter;

a receiver; and

an interconnect coupled to the transmitter and the receiver;

wherein the receiver includes an equalization circuit comprising:

~~an~~ a CMOS amplifier;

a CMOS gain circuit coupled to an output of the CMOS amplifier, the CMOS gain circuit to provide at least two gain values in response to the output of the CMOS amplifier; and

a control circuit to provide one of the at least two gain values as an output.

18. (Currently Amended) The system as claimed in claim 17, wherein the CMOS gain circuit includes at least two equalization circuits each providing a respective one of the at least two gain values.

19. (Currently Amended) The system as claimed in claim 18, wherein the at least two equalization circuits are coupled in series to the output of the CMOS amplifier.

20. (Currently Amended) The system as claimed in claim 18, wherein each of the at least two equalization circuits includes an RC filter.

21. (Canceled)

22. (Currently Amended) The system as claimed in claim 21, wherein the CMOS gain circuit includes at least two equalization circuits each providing a respective one of the at least two gain values.

23. (Currently Amended) The system as claimed in claim 22, wherein the at least two equalization circuits are coupled in series to the output of the CMOS amplifier.

24. (Currently Amended) The system as claimed in claim 23, wherein each of the at least two equalization circuits includes an RC filter.

25. (Original) The system as claimed in claim 17, wherein the control circuit includes a DC feedback circuit and the output provided by the control circuit is selected in response to the DC feedback circuit.

26. (Original) The system as claimed in claim 25, wherein the DC feedback circuit uses DC balance to help select the output.

27-32. (Canceled)

33. (New) The apparatus of claim 1, wherein the apparatus comprises an equalizer to equalize inter-symbol interference generated by frequency dependent loss characteristics of printed circuit board traces.

34. (New) The apparatus of claim 1, wherein the apparatus comprises an equalizer to equalize inter-symbol interference generated by frequency dependent loss characteristics of high speed point-to-point interconnects between two integrated circuits.

35. (New) The system of claim 17, wherein the transmitter and the receiver are each integrated circuits on a printed circuit board and the interconnect is a high speed interconnect on the printed circuit board, wherein the equalization circuit is to equalize inter-symbol interference generated by frequency dependent loss characteristics of printed circuit board traces.

36. (New) The system of claim 17, wherein the transmitter and the receiver are each integrated circuits on a printed circuit board and the interconnect is a high speed interconnect on the printed circuit board, wherein

the equalization circuit is to equalize inter-symbol interference generated by frequency dependent loss characteristics of the high speed point-to-point interconnect.